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| 09/873,875 | 06/04/2001 | Christophe de Dinechin | 10011596-1 | 5117 |

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| EXAMINER | |
|---|---|
| VO, LILIAN | |
| **ART UNIT** | **PAPER NUMBER** |
| 2195 | |

DATE MAILED: 04/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/873,875 | DE DINECHIN ET AL. | |
| | Examiner | Art Unit | |
| | Lilian Vo | 2195 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *02 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1 - 26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. Claims 1 – 26 are pending.

### *Claim Objections*

2. **Claim 25** is objected to because this newly added claim also stated "original" which examiner believes that is a typographical error.

Appropriate correction is required.

### *Claim Rejections - 35 USC § 101*

3. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

**4.** Claims 1 – 11, 22 – 26 are rejected under 35 U.S.C. 101 because they are directed to non-statutory subject matter.

**5. Claims 1 – 11 and 23 – 26** are directed to method steps, which can be practiced mentally in conjunction with pen and paper, therefore they are directed to non-statutory subject matter. Specifically, as claimed, it is uncertain what performs each of the claimed method steps. Moreover, each of the claimed steps, inter alia, saving, preventing, restoring, using, can be practiced mentally in conjunctions with pen and paper. The claimed steps do not define a machine or computer implemented process [see MPEP 2106]. Therefore, the claimed invention is directed to non-statutory subject matter. (The examiner suggests applicant to change

"method" to "computer implemented method" in the preamble to overcome the outstanding 35 U.S.C. 101 rejection).

6. **Claim 22** lacks utility and is non-statutory as not being tangibly embodied in a manner to as to be executable.

***Claim Rejections - 35 USC § 103***

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1 – 5, 9, 11 – 16, 20, 22 and 24 - 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bugion et al. (US 6,496,847, hereinafter Bugion).

9. Regarding **claims 1 and 9,** Bugion discloses a method of switching context on a processor (col. 4, lines 52 – 61), the method comprising:

saving and restoring the context under software control to memory (col. 4, lines 46 – 48, col. 11, lines 13 - 15: instructions to be carried out upon occurrence of exception or interrupt. Col. 17, lines 20 – 21. Col. 4, lines 52 – 61: switching from and to between the HOS context and the VMM context is then carried out in the driver and in the virtual machine monitor, respectively. Col. 11, lines 30 – 52: any available memory space may be used to save context and actual storage and retrieval may be accomplished using any known technique); and

preventing the processor from changing the context while the context is being saved (col. 11, lines 30 – 52: total switch preferably first saves the state before setting it according to the target context in order to facilitate the inverse operation. Col 17, lines 18 – 21: ensure that no interrupts occur during the switch).

Bugion did not clearly disclose the context is being saved and restored using an inconsequential register as temporary storage before switching. Instead, Bugion discloses that any available memory space may be used to save the information and actual storage may be accomplished using any known technique (col. 11, lines 39 – 41). It is obvious for one of an ordinary skill in the art, to relate the available memory with any type of memory such as the inconsequential register because inconsequential register is just another type of storage or memory that is not used by the host OS at the time of the interruption according to applicant's specification page 6, lines 6 – 7. It would have been obvious for one of an ordinary skill in the art, at the time the invention was made to modify Bugion's system to particularly use the inconsequential register as the available memory for storage and still able to perform the intended functions equally well.

10. Regarding **claim 2,** Bugion disclose the inconsequential register (available memory) is used as a temporary storage in lieu of a privileged register (col. 11, lines 62 – 67: context refers to state that is set and restored during the switching including the privileged registers).

11. Regarding **claim 3**, Bugion discloses the context is saved at a predetermined interruption point (col. 10, lines 31 – 48, col. 17, lines 6 – 21).

12. Regarding **claim 4,** Bugion discloses the context is switched between a host operating system and a virtual machine application (col. 4, lines 52 – 61: switching from HOS context to VMM context. Col 11, lines 30 – 52), the virtual machine application controlling the context switch (col. 11, lines 30 – 52: VMM handles directly all exceptions and interrupts that occur while executing in the VMM context. Col. 12, lines 20 – 24: the VMM completely takes over the machine and only voluntarily relinquishes control to the HOS).

13. Regarding **claim 5,** Bugion discloses the inconsequential register is used to pass information to the virtual machine application (col. 11, lines 30 – 52: total switch saves HOS context to any available memory space and changes the address space to be mapped into the VMM context. Col. 16, lines 45 - 61).

14. Regarding **claim 24,** as modified Bugion discloses the inconsequential register includes storing an address, the address indicating a memory location at which the context will be saved (col. 11, lines 41 – 46, col. 14, lines 4 – 6).

15. Regarding **claim 25,** as modified Bugion discloses the inconsequential register does not store context a predetermined interruption point (col. 8, lines 36 – 39, col. 16, lines 36 – 42).

16. Regarding **claim 26,** Bugion discloses the context is stored in memory other than the inconsequential register (col. 11, lines 30 – 52: any available memory space may be used to save context and actual storage).

17. **Claims 11 – 16, 20 and 22** are rejected on the same ground as stated in claims 1 – 5 and 9 above.

18. Claims 6, 17 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bugion et al. (US 6,496,847, hereinafter Bugion) as applied to claims 1 and 12 above, in view of Applicants' admitted prior art.

19. Regarding **claims 6 and 17,** Bugion did not clearly disclose the context switched is using an IA-64 processor. However, Bugion discloses the process of total context switching (col. 11, lines 30 – 52) that is done in virtual machine monitor (col. 4, lines 52 – 61), in which VMM can also provide architectural compatibility between different processor architectures by using known technique (col. 2, lines 21 – 36). Furthermore, an IA-64 processor is considered a well-known architecture as disclosed in Applicants' admitted prior art (specification page 1, paragraph 4). It would have been obvious for one of an ordinary skill in the art, to implement Bugion's system with an IA-64 processor because Bugion switches total context that uses VMM which capable of providing architectural compatibility between different processor architectures (col. 2, lines 21 – 36).

20. Regarding **claim 23,** Bugion did not clearly disclose the content of the inconsequential register is corrupted during the context switch. Nevertheless, this limitation has been disclosed in AAPA as a well-known feature in which certain registers might be corrupted by context switching process (specification page 1, paragraph 4). It would have been obvious for one of an ordinary skill in the art, at the time the invention was made, to incorporate this knowledge with Bugion to be aware of the issue, particularly when perform context switch in an IA-64 processor so that current state of the process can be properly reserved and restored when its execution is resumed again.

21. Claims 7, 8, 10, 18, 19 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bugion et al. (US 6,496,847, hereinafter Bugion) as applied to claims 6, 9, 17 and 20 above, in view of Yamaura et al. (US. Pat. Application Publication 2001/0008563, hereinafter Yamaura).

22. Regarding **claims 7 and 8,** Bugion did not clearly disclose the temporary storage includes caller-save register or branch register. Nevertheless, Yamaura discloses a system that use link register (caller-save register) for holding an address of a source from which a subroutine call is made and LI and LN registers (branch register, caller-save register) for holding branch destination addresses at a time of IRQ (page 6, paragraph 0110 and page 12, paragraph 209, page 5, paragraph 0082). It would have been obvious for one of an ordinary skill in the art, at the time the invention was made, to particularly implement Bugion's system with Yamaura's teaching

with the use of link register and/or branch register as a storage to hold the addresses of the current context information so that data can be accessed more quickly.

23. Regarding **claim 10,** Bugion did not clearly disclose the context is restored by using a branch register to perform an indirect branch. Nevertheless, Yamaura disclose a system that use a plurality of registers for storing data to undergo operation processing which can be freely written/read to/from the registers (page 5, paragraph 0082). Furthermore, Yamaura discloses that LI and LN registers (branch register, caller-save register) are used for holding branch destination addresses at a time of IRQ (page 6, paragraph 0110 and page 12, paragraph 209, page 5, paragraph 0082). It would have been obvious for one of an ordinary skill in the art, at the time the invention was made, to particularly implement Bugion's system with Yamaura's teaching with the use of branch register as a storage to hold the destination addresses at a time of IRQ when restoring the context so that processing can be resumed from last interrupt efficiently and quickly.

24. **Claims 18, 19 and 21** are rejected on the same ground as stated in claim 7, 8 and 10 above.

***Response to Arguments***

25. Applicant's arguments filed 12/2/04 have been fully considered but they are not persuasive for the reason set forth below.

26. On page 7, 2nd paragraph, applicant argues in essence "Bugion et al. don't indicate whether context-switching is done under hardware control or software control". Applicant is directed to col. 4, lines 46 – 48 and col. 11, lines 13 – 15, col. 17, lines 20 - 21. Bugion has specifically taught the use of instructions to be carried out upon the occurrence of interrupt or exception. Therefore, this argument is moot.

27. On page 7, 3rd paragraph, applicant argues in essence "Bugion et al. don't teach or suggest preventing the processor from changing the context while the context is being saved". However, the processor MUST be prevented from changing the context while the context is being saved because "the total switch also changes the address space so that the host operating system's address space does not need to be mapped into VMM's address space" (col. 11, lines 41 – 44). "Total switch preferably first saves the state before setting it according to the target context in order to facilitate the inverse operation" (col. 11, lines 50 – 52). Furthermore, Bugion discloses "the total switch routine uses known techniques to ensure that no interrupts occur during the switch" (col. 17, lines 18 – 21). In other words, the processor is not loading/setting the target context (changing) until after it has saved the current context. Therefore, this argument is moot.

With respect to applicant's argument that Bugion does not teach or suggest disabling the interrupts (page 7, 3rd paragraph, last two lines). Applicant is arguing a feature of the invention not specifically stated in the claim language, which is improper. Claim subject matter, not the specification, is the measure of invention. Limitations in the specification cannot be read into

the claims for the purpose of avoiding the prior art. In re Self, 213, USPQ 1,5, (CCPA 1982; In re Priest, 199 USPQ 11,15 (CCPA 1978).

28. On page 7, 4th paragraph, applicant argues in essence "Bugion et al. don't teach or suggest the use of an inconsequential register during context switching. According to paragraph 21 of the application, an inconsequential register is a register that is not used at a predetermined interruption point (PIP)".

With respect to the term "inconsequential register", the specification disclosed that it was used as a temporary storage. Since the specification did not provide a precise meaning of an inconsequential register beside it's a type of storage and that it is "a register that is not used at a predetermined interruption point (PIP)", the claim must be given its broadest reasonable interpretation. This means that the words of the claim must be given their plain meaning unless applicant has provided a clear definition in the specification (See MPEP 2111.01.) In this case, the inconsequential register is just storage or memory. As such, Bugion teaches that any memory space may be used to save the context. Furthermore, the specification states that the inconsequential register does not store context at a PIP. This statement does not mean a register is not a memory or cannot be a storage. Bugion did not mention that the context being saved to memory is being stored at PIP. Therefore, this argument is moot.

Additionally, applicant is directed to Shaylor (US 6,408,325) to see support for which register is a form of memory (col. 1, lines 22 – 24).

Applicant is also directed to Borkenhagen et al. (US 6,697,935) to see support for which context when switch is saved to a register (abstract, col. 5, lines 40 – 45).

29. In response to applicant's argument (page 7, last paragraph – page 8, 1st paragraph, line 3) that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the motivation can be found in the knowledge generally available to one of an ordinary skill in the art. It would have been obvious for one of an ordinary skill in the art, at the time the invention was made to modify Bugion's system to particularly use the inconsequential register as the available memory for storage and still able to perform the intended functions equally well.

With respect to applicant's remark that any available memory is vague and offers no reasons for identifying registers that are inconsequential and then using the inconsequential registers (page 8, 1st paragraph, last sentence), the examiner disagrees. The authoritative dictionary of IEEE standards terms defined the terms 1) memory as a storage and 2) the register as a storage location or high-speed storage location as one would use memory. Furthermore, the term inconsequential according to the dictionary means not important. In other words, inconsequential register merely means a temporary storage and/or unspecified, general storage. Therefore, it is reasonable and proper to relate any available memory as disclosed by Bugion with any type of memory such as the inconsequential register because inconsequential register is

just another type of storage or memory and still able to perform the intended functions equally well.

30. With respect to applicant's remark, regarding the two unresolved issues (page 8, last two paragraph), they have been addressed during the telephone interview on 12/1/04. Applicant is directed to the rejection and/or response to arguments above for additional details and/or supports.

As per the remarks that "the examiner appears to have stated that the process of switching context is what prevents the context from being changed", the examiner disagrees. Applicant appears misunderstood the examiner's point during the telephone interview. Applicant is again directed to the response to arguments as state above for additional details and/or support.

31. With respect to applicant's argument that "claim 1 doesn't recite storing context in an consequential register, but rather using the inconsequential register to store context" (page 9, 2nd paragraph), the examiner is unable to identify the differences between storing context in a consequential register and using the consequential register to store context. In other words, the examiner interpret and understand they both means the context can be saved to the consequential register or the consequential register is used to save the context. MPEP 2111.01 states that the claim must be given its broadest reasonable interpretation. Therefore, this argument is moot.

32. With respect to applicant's argument regarding claim 1 during the telephone interview, which are the new issues in newly added claims 23 – 25 and 5th paragraph on page 9, applicant is

again arguing a feature of the invention not specifically stated in the claim 1 language, which is improper. Claims subject matter, not the specification, is the measure of invention. Limitations in the specification cannot be read into the claims for the purpose of avoiding the prior art. In re Self, 213, USPQ 1,5, (CCPA 1982; In re Priest, 199 USPQ 11,15 (CCPA 1978). In this cases, the new issues in claim 23 – 25 and page 9, 5th paragraph cannot be read into claim 1 for the purpose of avoiding the prior art. Therefore, this argument is moot.

33. Applicant's arguments (page 10, 2nd paragraph) fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claim defines a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references.

***Conclusion***

34. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lilian Vo whose telephone number is 571-272-3774. The examiner can normally be reached on Monday - Thursday, 7:30am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lilian Vo
Examiner
Art Unit 2195

lv
March 30, 2005

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